September 1999 • NREL/SR-520-26834

Subcontractor Report

Silicon-Film™ Solar Cells by a Flexible Manufacturing System

Annual Subcontractor Report
16 April 1998—31 January 1999

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AstroPower, Inc.
Newark, Delaware

National Renewable Energy Laboratory

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Table of Contents

Figures

Tables

Executive Summary

AstroPower is developing a manufacturing process for Silicon-Film™ solar cell production under an NREL-administered PVMaT cost-share program. This document reports on results from the first phase of a three phase effort. Progress is reported on the development of new procedures and equipment for in-line wet chemical processes, metallization processes, sheet fabrication, solar cell processing, module assembly, solar cell test, metallurgical-grade silicon purification, and recycling of Silicon-Film™ sheet materials. Future concepts and goals for the Silicon-Film™ process are also discussed.

During the time period of this effort, AstroPower brought online a new manufacturing facility (the Pencader facility) for the manufacture of Silicon-Film™ solar cells and modules. The new 60,000 sq. ft. factory is located in Newark, DE. The facility has a capacity of 9 MW.

A major technical goal of this effort is the elimination of batch production processes in AstroPower's solar cell process. New processes are being developed to accommodate large area Silicon-Film™ planks in an in-line, continuous manner. During this first phase, one cassette-based process was replaced with an in-line, continuous belt process. Two other processes have production equipment under development to achieve the same result.

AstroPower is developing a size-based family of Silicon-Film™ products to address the full range of off-grid applications. Processing the large-area Silicon-Film™ plank will allow a large range of solar cell (and thus module) configurations while maintaining a single high-volume manufacturing configuration through the solar cell line. During this phase 30 x 30 cm^2 AP-900 prototype solar cells were fabricated using a deHaart screen printer. This demonstrates the compatibility of large-area Silicon-Film™ material with standard screen printing equipment. Large belt furnaces were installed and commissioned for use in belt-gettering, belt-diffusion, and front and back metallization process steps. These significantly wider belt furnaces (36-inch wide) have greatly increased throughput in all of these processes and can easily accommodate the large-area Silicon-Film™ planks.

Production throughput levels of Silicon-Film™ AP-225 solar cells were increased by the development and improvement of continuous in-line gettering and diffusion processes. These processes have increased throughput and lead to increases in diffusion length, current generation, fill factor and efficiency of production solar cells. Costs for Silicon-Film™ modules have been reduced through the design of a new, lower cost, junction box for all AstroPower module products. This junction box is in the process of being UL approved. A Spire stringer-tabber was installed and commissioned to further mechanize module assembly and reduce costs. A new solar cell tester was designed, constructed and commissioned. This flexible system is capable of handling and testing large-area cells up to 8" (AP-400).

Introduction

Figure 1. Silicon-Film™ sheet material.

The Silicon-Film™ process is presently in production at a new 9 MW nameplate capacity manufacturing facility which started production in 1998. The present process is based on a 240 cm^2 solar cell (AP-225). Efficiencies exceeding 12% have been measured for the AP-225. Small, laboratory-scale devices have demonstrated efficiencies as high as 16.6%.

The approach and accomplishments in this report focus on the concept of "flexible" solar cell manufacturing. This involves continuation of engineering efforts to generate large areas of high-quality Silicon-Film™ sheet material at high speeds and to implement new cassette-less, in-line processing equipment for solar cell manufacture.

The areal dimensions of Silicon-Film™ wafers and solar cells increased from 10 x 10 cm^2 to 15 x 15 cm^2 during the AstroPower PVMaT-4 program. Solar cell fabrication processes are now being designed and developed within the AstroPower PVMaT-5 program to process large-area (30 x 120 cm^2) Silicon-Film™ planks into solar cells.

During Phase I of this PVMaT program, significant progress has been made in developing large-area, in-line process machines for AR coating, belt gettering, belt diffusion, hot caustic surface etching, and diffusion oxide etching. A large area, high-speed solar cell test/sort machine was designed, fabricated and commissioned for the new manufacturing facility. Large-area semi-automatic screen printers and collocators were commissioned along with 36"-wide contact firing furnaces. Further metallization improvements are expected during the next two phases of the AstroPower PVMaT effort, and a new Silicon-Film™ sheet generation machine with twice the throughput of the present machine will be constructed during Phase II based on designs established during the Phase I effort.

Approach

There are three basic development areas that are involved in transferring Silicon-Film™ technology from the laboratory to the factory:

- Optimization of the sheet generation process -- high-speed, high quality, and large areas are desired.
- Optimization of the solar cell fabrication sequence to achieve high efficiency with large areas. These processes must be compatible with manufacturing and should be in-line and continuous rather than batch-mode.
- Integration of these developments in an industrial setting by the generation and sale of significant quantities of solar cells.

To achieve these broad objectives, AstroPower directed 1998 PVMaT development efforts into the following distinct tasks:

Task 1.	In-Line Wet Processing.
Task 2.	Continuous Metallization.
Task 3.	New High-Throughput Sheet Machine.
Task 4.	Solar Cell Efficiency and Module Cost-Reduction Improvement.
Task 4A.	Increased Efficiency of Production Solar Cells.
Task 4B.	Metallurgical-Grade Silicon for Solar Application.
Task 4C.	Reduced Silicon Consumption through Recycling.

Results

In-Line Wet Processing

The goal of this task is to develop a set of production tools capable of processing large sheets of Silicon-Film™ material using a cassette-less in-line approach. In Phase I, we achieved the following results.

- Purchased and installed an in-line Rinser-Dryer system in the new production facility. Use of this apparatus has resulted in a significant increase in throughput and quality compared to cassette-based spin-dry systems.
- Fabricated and evaluated a first-generation prototype hot caustic etching system. The results of this effort have formed the basis for a rigorous understanding of the chemistry of the $NaOH\text{-}Si\text{-}H_2O\text{-}Si_xO_y$ system and the suitability of various wetted materials and components exposed to hot, concentrated caustic solutions. In 1999, a second-generation prototype will be designed and assembled to further develop this process.
- Evaluated a number of potential in-line dilute HF “deglazing” systems for removal of diffusion oxides. We are currently in the final selection and specification process and expect to install and evaluate this system in 1999. After the evaluation process, it is expected that this machine will be directly transferred to production.

Continuous In-line Wafer Rinse-Dry System

To investigate the in-line wafer handling approach, a continuous wafer rinser-drier was specified and procured. This equipment is based on standard modular units consisting of load, rinse, dry, and unload sections. Each module is able to stand alone, but is bolted together to form a system. The results achieved with this continuous, in-line rinser-dryer system have been impressive. Wafers travel through the system at a speed of about 50 inches per minute. At this speed with maximum loading, the throughput of this system is over 2500 AP-225 wafers per hour. For comparison, a spin drier would take more than ten minutes to dry four cassettes (or 100 wafers).

Based on the performance and reliability of this initial rinser-dryer system with production quantities of AP-225 Silicon-Film™ wafers, we have concluded that this type of in-line wet process equipment is the correct path for further wet process development. Large-area wafers or even full-width planks can also be processed with this type of equipment.

Continuous In-Line Pre-Getter Surface Preparation

Several cassette-based chemical process steps, including surface preparation prior to the gettering process and oxide strip following junction diffusion, exist in the current solar cell production line. These labor intensive chemical processes require the wafers to be loaded into cassettes, moved between chemical tanks by hand, dried in cassettes, and then unloaded. The maximum wafer size is limited by the cassette size, and the total throughput is limited by the tank size. Also batch processes such as this are difficult to control, and the use of cassettes in processing reduces the liquid flow to the wafers and at times results in uneven etching and cleaning at the edges.

The implementation of an in-line wet chemical processing system would eliminate many of the limitations discussed above. Such a system would be capable of handling wafers of various sizes, even uncut Silicon-Film™ planks. Operator exposure to chemicals would be minimized by a completely enclosed system where dry wafers are loaded for processing and completely rinsed and dried before being unloaded from the system. The composition of the process solutions would be maintained within operating limits by in-line monitoring and control. Such control would reduce raw material use and waste stream volume. Throughput of the in-line system would no longer be limited by tank size and the time consuming cassette loading and unloading operations. Total processing time would be further reduced by the more efficient cassette-less rinsing and drying steps.

Experimental Determination of Sodium Hydroxide and Silica Concentration

Determination of both NaOH and SiO_2 concentrations in etch solution is a critical first step to etch bath characterization, which is necessary for process automation, therefore several analytical techniques have been investigated. Gravimetric, titration and colorimetric methods have been considered for silica concentration determination. The gravimetric method was found to be unreliable because silicates can precipitate out as silica, silicate polymers (gels), or in many other forms of hydrated silica. The titration method, if performed carefully, is extremely

accurate. Both sodium hydroxide and silica concentration of a standard solution were determined within 0.5wt. %. A drawback to this procedure is the time required for titration (one or more hours if done by hand). Two colorimetric methods for determining silica concentration were evaluated. Both methods involve the conversion of silica to a colored complex and measurement of the intensity of light of a specific wavelength transmitted through the sample. The intensity of the analyzed sample is related to the total silica concentration. The colorimetric method is less accurate, but significantly faster, than the titration method.

The analytical techniques developed for SiO_2 and NaOH determination were applied to etch tanks for monitoring purposes. The concentration of NaOH and SiO_2 both increased with the number of wafers etched (Figure 2). The increase in silica concentration was expected and corresponded to theoretical values. The increase in sodium hydroxide concentration was not expected. Further experiments were conducted, from which it was determined that NaOH refresh, periodic addition of sodium hydroxide to the etch tank to maintain constant NaOH concentration during etching, exceeded NaOH consumption. As a result of this work sodium hydroxide usage was cut in half with further reductions expected.

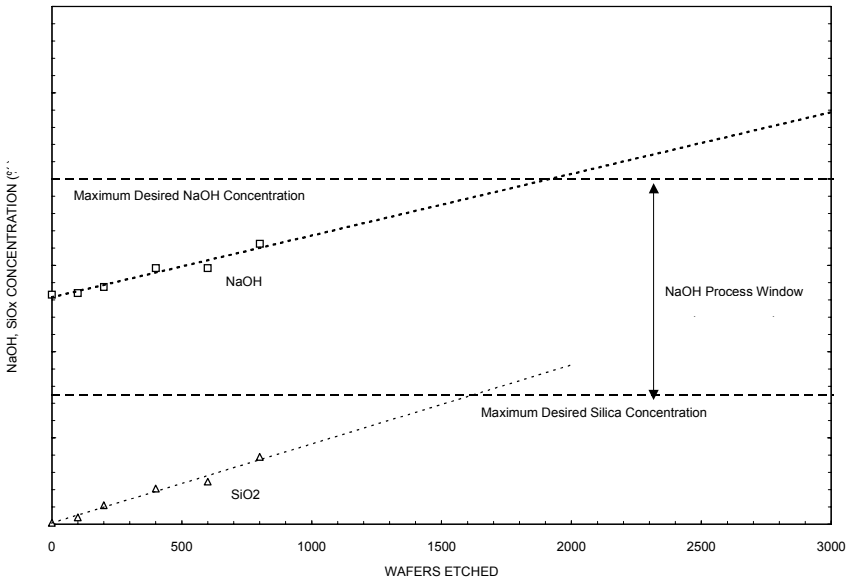


Figure 2. Composition of production etch bath.

Etch Rate Determination

The etch rate of Silicon-Film^{TM} wafers in sodium hydroxide was investigated in order to design a production-scale in-line etch machine. Such information is crucial in determining etch time and machine length. Laboratory-scale experiments were conducted to determine the factors affecting etch rate.

It was suspected that increased silica concentration reduced the silicon etch rate in sodium hydroxide. Experiments, the results of which are shown in Figure 3, were conducted to test this model. Based on the experimental results the etch rate does not appear to be strongly influenced by silica concentration at these levels.

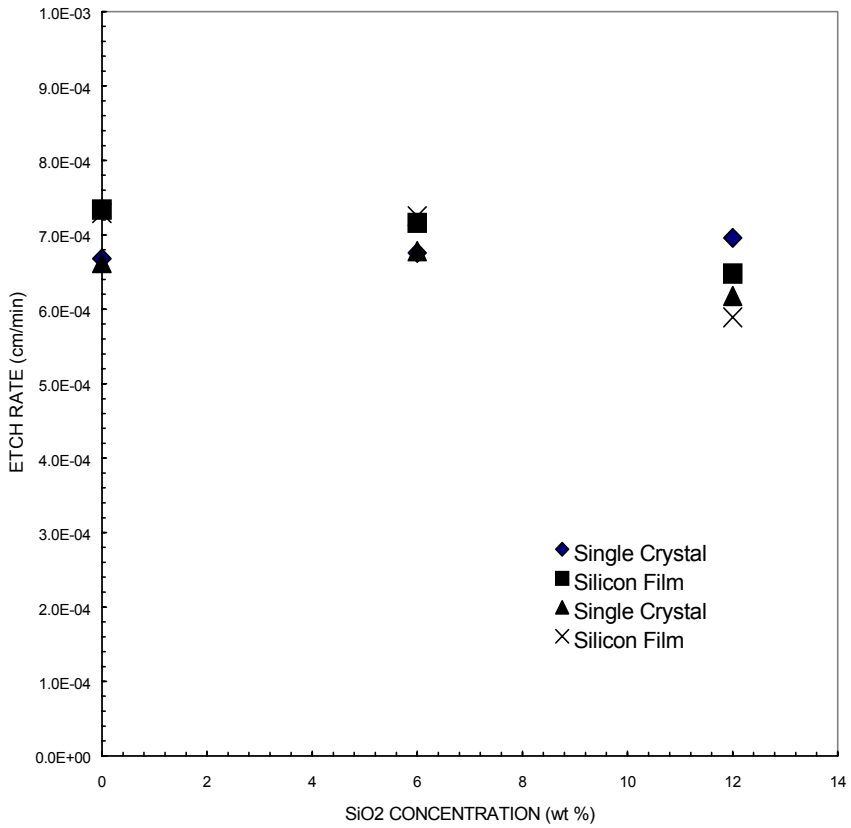


Figure 3. Etch rate of silicon versus silica concentration in NaOH solutions.

Since silica concentration was found not to have a significant influence on etch rate, the relationship between etch rate and NaOH concentration was investigated. Another small-scale etch rate experiment was performed. Results similar to the KOH/Si etch system were expected. The KOH/Si system was presented by Seidel, *et al.* [1] where, for a constant temperature of 72°C, the etch rate of silicon in KOH:H_2O solutions dropped off significantly for KOH concentrations greater than 30 wt%. However, in the same reference, Seidel demonstrated that the etch rate dependence on temperature is stronger than its dependence on hydroxide concentration. For this reason, the expected drop off in etch rate at high NaOH concentrations was not observed due to temperature fluctuations in the reaction vessel. Therefore, in order to control etch rate in production tanks, the temperature needs to be strictly controlled while the sodium hydroxide concentration can be allowed to fluctuate in a specified range.

In-line Pre-getter Etch

We constructed and evaluated the first prototype of the in-line etch system. This experimental model has the capacity to hold one AP-225 wafer during the caustic etch step of the surface preparation process. Rinsing and neutralization steps are performed manually.

Experiments were conducted using this prototype to determine the minimum etch time required for acceptable electrical results. Groups of wafers were etched for various time

intervals at constant etch temperature. These samples were then processed into solar cells using standard manufacturing processes. Figure 4 shows a sample of the test results where power has been normalized against the average power of standard solar cells, and the etch interval was normalized with respect to standard production etch time. These data show a significant increase in solar cell electrical performance as the etch time increases. However, for etch times more than twice the standard production time, performance begins to level off.

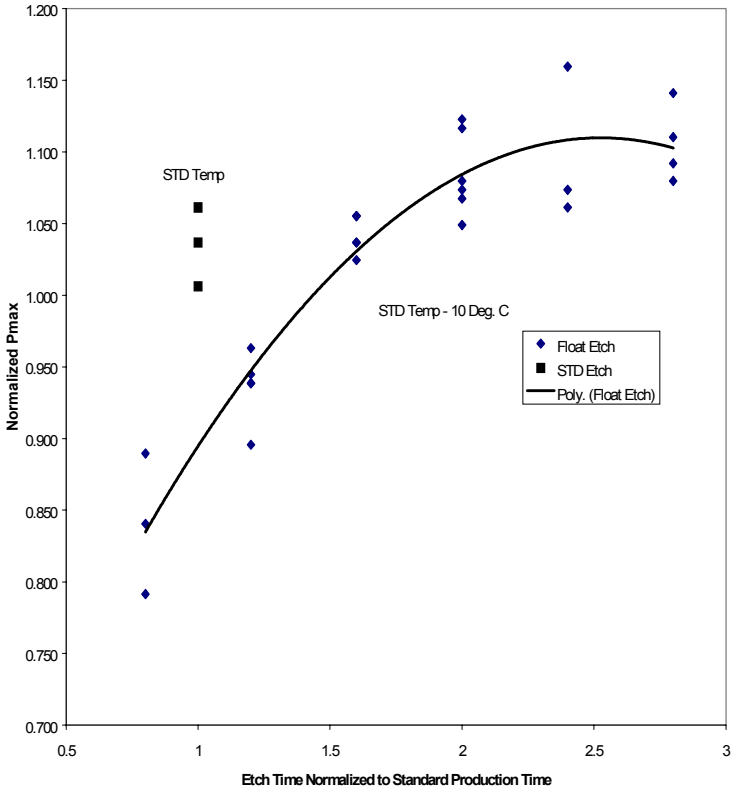


Figure 4. Normalized power vs. etch time.

We have begun the design of the next prototype etching system, which will be used to develop the wafer transport system. It will be a single-track system (one wafer wide) and consists of two sections: etch and rinse. All of the sumps, pumps and filters will be self-contained. Two additional process steps consisting of a spray rinse and dry can be added. These modules are the same as those which were successfully demonstrated by the previously mentioned rinser-dryer system.

In-Line Diffusion Oxide Deglaze System

During the diffusion process a thin layer of phosphorus-doped silicon dioxide grows at the surfaces of the wafers. This oxide must be removed prior to the contact metallization steps; usually this is accomplished by briefly etching the wafers in a dilute hydrofluoric (HF) acid solution. At present, the etching process is cassette based and performed in wet process tanks in a chemical fume hood. Once the diffusion oxide is etched, the wafers are unloaded from the cassettes so that they can proceed to the next process step.

Changing from a batch to in-line diffusion oxide strip is expected to significantly improve the process and reduce both material use and the waste stream volume. Such in-line systems also minimize operator exposure to process chemistries due to the fact that most modules are self-contained. Because of the modular design approach, this type of equipment is adaptable for silicon plank as well as solar cell processing. A diffusion oxide etching system for Silicon-Film™ wafers might consist of an HF-etch process module, a rinse module, and a dry module, along with any required loader and unloader sections. Since the in-line chemical etch system is cassette-less, we expect labor cost to be reduced and throughput to be increased. In the following year AstroPower will purchase such a unit and begin experiments with Silicon-Film™ wafers.

Continuous Metallization

The goal of this task is to assess technologies that are suitable for applying front and back contact metallization to Silicon-Film™ with the intent of handling larger solar cells and planks. Cutting the plank to final solar cell size will be moved to a much later step in the process sequence. Much of the work carried out in Phase I focused on equipment and inks for screen printing. Progress also occurred with the development/deployment of new contact firing furnaces, belt-loading collocators, ink formulations, screen printing screens, and with various solar cell sizes.

AstroPower is developing a size-based family of Silicon-Film™ products to address the full range of off-grid applications. As illustrated in Figure 5, from the large area Silicon-Film™ "master solar cell" stems the unique capability to produce a large range of solar cell (and thus module) configurations while maintaining a single high-volume manufacturing configuration through the solar cell line.

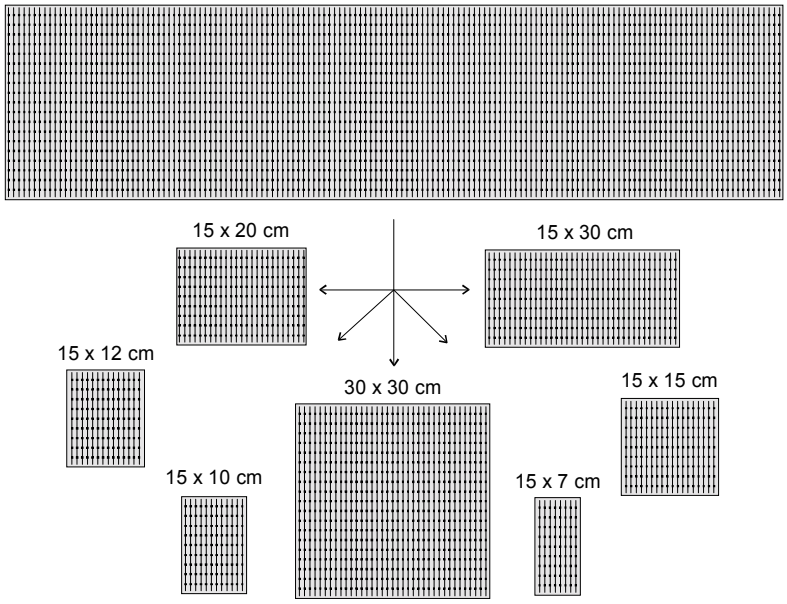


Figure 5. 30 cm x 120 cm "master solar cell" and product flexibility.

During Phase I, we achieved the following results in Task 2.

- Screen printed a 30 x 30 cm^2 AP-900 prototype solar cell using a deHaart screen printer. This demonstrates the compatibility of large-area Silicon-Film™ material with standard screen printing equipment.
- Installed and commissioned 36-inch wide belt furnaces in both production facilities for high-temperature cell processing. These furnaces are used for belt-gettering, belt-diffusion, and front and back metallization process steps. These significantly wider belt furnaces have greatly increased throughput in all these processes.
- Installed and commissioned semi-automatic screen printers with furnace-belt-load collocators that are matched to the 36-inch wide belt furnaces.
- Investigated new contact metallization ink formulations.
- Investigated new types of screens for printing fine lines.
- Designed metallization patterns for the "family" of proposed Silicon-Film™-based products.
- Evaluated and assessed other potential metallization technologies.

Large-area belt furnaces

Prior to this contract, the widest infrared belt furnace available for solar cell processing was 24 inches wide and the fastest screen printers were supplied with collocators (belt loaders) matched to this 24 inch width. Our analysis has shown that, for an in-line process such as plank production or metallization firing, increasing the width of the system yields a significant improvement in process costs.

Discussions with a furnace manufacturer resulted in the conclusion that it was feasible to produce a 36-inch wide furnace and that the capital cost of a wider furnace is not significantly higher than a 24 inch system. During Phase I, we developed a specification for a 36-inch wide metallization firing furnace. Four furnaces have been purchased and installed in AstroPower facilities.

Screen printers are supplied with collocators which are matched to the width of the process furnace. The widest collocator available before Phase I was 24 inches. Two screen printer manufacturers were asked to provide screen printers with new, wider collocators to match the 36 inch furnaces. One manufacturer agreed to re-design an existing collocator system and integrate it with a standard screen printer. Two of these wide-collocator screen printers were purchased and commissioned in the Pencader facility.

Low contact resistance ink

We have begun to work with an ink manufacturer on new front contact inks that would result in lower contact resistance. Our initial meeting took place at the end of Phase I, and a work plan was developed. The manufacturer has agreed to provide experimental silver front contact inks (200 gm samples) to AstroPower. In return, AstroPower will test the inks by

fabricating solar cells with different time-temperature sintering schedules and will provide IV data, particularly series resistance information.

High resolution screen printing

Shadowing by the grid metallization is a significant loss mechanism for screen printed solar cells. Shadowing is a function of the wafer surface characteristics, the metal ink formulation, the screen printer settings, the screen pattern, and the screen itself. During Phase I we investigated the effect of calendered, elliptical rather than round wire, screens on gridline width and shadowing. Calendered screens offer the possibility of printing taller and finer lines on the front surface of solar cells, reducing both shading and R_s losses.

An initial comparison between the screen currently used by AstroPower and the calendered screen was performed. The experiment involved approximately 100 AP-225 solar cells. All devices were processed together up to the front-contact step. Half of the solar cells were then printed using the standard screen and the other half were printed using the calendered screen. Only grid geometry was examined in this experiment. The results are given in Table 1.

Table 1.
Comparison of gridline geometries on AP-225s
using the standard production front-contact screen
and the calendered front-contact screen.

	Average Gridline Width (μm)	Average Gridline Height (μm)
Standard	291	16
Calendered	250	19
% Change	-8.1%	+18.8%

The calendered screen demonstrated an improvement in overall gridline geometry. No power data was collected for these cells. Performance modeling estimates that the decreases in grid resistance and grid shading due to the new geometry will result in a 20 mW increase in power.

Grid design for the family of Silicon-Film™ products

Using recently developed power-loss models, optimized front-contact grid parameters have been established for a family of Silicon-Film™ products. The cell dimensions, number of busses and number of grid lines are given in Table 2. All of the grid designs incorporate 16 μm grid and buss height, 250 μm grid widths, and 2 mm buss widths. These values, along with sheet resistivity, junction depths, bulk resistivities and thicknesses, are in accordance with AP-225 device analysis and present manufacturing capabilities in AstroPower's two production facilities. All rectangular devices utilize bussbars along the short axis.

30Table 2.
Grid design parameters for a family of Silicon-Film™ based solar cell products

Cell Dimensions (cm^2)	P_{max} (Watts)	P_{loss} Grids (%)	P_{loss} Emitter (%)	P_{loss} Bulk (%)	P_{loss} Total (%)	Busses	Grids
30 x 30	9.7	0.40	2.58	2.09	5.07	6	78
15 x 30	5.2	0.66	1.36	2.12	4.14	4	54
15 x 20	3.4	0.62	1.94	2.08	4.64	3	45
15 x 15	2.5	0.87	2.42	2.08	5.37	2	40
15 x 12	2.0	0.76	1.95	2.14	4.85	2	36
15 x 10	1.7	0.78	1.96	2.13	4.87	2	30
15 x 7	1.2	0.72	1.51	2.15	4.38	2	24

Recently, AstroPower has begun manufacturing other Silicon-Film™-based modules utilizing smaller solar cells. These compact designs are designed for remote-applications markets where low-power, high-voltage requirements supersede high current needs. Flexibility in the Silicon-Film™ manufacturing process has allowed these modules to be built with relatively little adjustment to solar cell and module production processes.

The larger 30 cm x 30 cm device was fabricated using AstroPower's laboratory facilities and continuous diffusion technology. The device fabrication sequence incorporated several post-growth enhancement techniques. The front gridlines were printed with a deHaart screen printer. This demonstrates the compatibility of large-area Silicon-Film™ material with standard screen printing equipment.

Through power-loss modeling, a family of Silicon-Film™ solar cells has been designed to meet the needs of grid-connected and off-grid PV arrays. AstroPower has already begun to explore the possibilities of these systems through creation of its APex™ module line. Continued utilization of the Company's flexible manufacturing system will allow these new solar cell sizes to be quickly produced and introduced to both the grid-connected and off-grid markets.

New High-Throughput Sheet Machine

The objective of the work performed under this task is to design a machine for the production of continuous silicon sheet at a speed twice that of the existing production machine. A modular approach was used in the design of the new higher-capacity system to meet the required production rate and final product cost goals.

The areal generation rate of the Silicon-Film™ sheet machine is determined by the product of the sheet pulling speed and the sheet width. A prototype Silicon-Film™ sheet generation machine produces a continuous sheet of silicon up to 38 cm wide. The Silicon-Film™ process for the machine presently in operation has been compared with the output realized by other sheet processes. The areal generation rate of the Silicon-Film™ sheet process is greater than the alternative sheet process with the highest areal generation rate, and five times greater than single crystal and cast polycrystalline silicon ingot methods.

The high areal generation rate of Silicon-Film™ sheet demonstrates the production rate advantage of the AstroPower process for producing large areas of crystalline silicon for processing into solar cells. There are other advantages as well. The thermal profiles employed in Silicon-Film™ growth lead to a reduction in thermal stress-induced material defects. In contrast, the large temperature gradients employed by other sheet generation techniques make it difficult to fabricate wide sheets (>10 cm). It is also well known that reducing thermally-induced stress in the material reduces breakage during solar-cell processing.

During Phase I, AstroPower completed the design of a Silicon-Film™ sheet machine. A series of tests were conducted on the present production machine that enabled the generation of data to drive the model for the high-throughput machine. A modular approach was employed to set the design for the three major process zones taking into account the specific thermal, chemical, electrical and mechanical attributes required to effect the process in each zone. Long-lead-time items have been identified and those parts have been ordered. The construction of the new machine will begin during Phase II.

Solar Cell Efficiency and Module Cost-Reduction Improvement

The goal of this task is to investigate process and characterization techniques to increase solar cell efficiency and lower module costs. In 1998, we achieved the following results.

- Developed an in-line AR coating system capable of coating large-area Silicon-Film™ solar cells.
- Evaluated the RF-PCD technique as a contactless material quality assessment tool. These results indicate that the RF-PCD technique is predictive of short-circuit current for devices with junctions. In 1999, we will continue to investigate the RF-PCD and other potential techniques with the goal of predicting the performance of as-grown Silicon-Film™ sheet material.
- Developed and improved continuous in-line gettering and diffusion processes to improve the diffusion length, current generation, fill factor, and efficiency of Silicon-Film™ AP-225 solar cells.
- Designed a new junction box for all AstroPower module products. This junction box is in the process of being UL approved. Higher current (over 10 A) bypass diodes for large-area solar cells and modules were identified. These diodes are in the process of being qualified.
- Installed and commissioned a Spire stringer-tabber system to further mechanize module assembly. This system was specified for application to AP-225 solar cell module production. Two large-area laminators were installed and commissioned. One manufactured by Spire and one by NPC.
- Designed, constructed, and commissioned a new automatic solar cell tester-sorter system for AP-225 solar cells. This flexible system is capable of handling and testing large-area cells up to 8” (AP-400).

The objective of the work performed under this Task is to develop advanced processing techniques that increase the efficiency of production Silicon-Film™ solar cells. This report summarizes work performed to enhance solar cell performance by optimizing production

processes related to module and device optics, the emitter or "blue response" of AP-225 solar cells and the bulk or "red response" of Silicon-Film™ material.

A detailed characterization of a typical AP-225 solar cell reveals that the short-circuit current is limited by losses in blue response, red response, and optical transmission. These loss mechanisms and associated issues can be further detailed as:

- Device optics: grid shading, AR coating, and surface morphology
- Blue response: junction formation, surface passivation, and metallization
- Red response: growth and post-growth improvement, characterization

To understand the potential improvements in short-circuit current, solar cell models have been developed to predict increases in current as improvements in each of the three areas are achieved. The calculated external quantum efficiencies for the production AP-225 solar cell are illustrated in Figure 6. This analysis shows that there is potentially a 1.4 A (26%) increase in the short-circuit current of an AP-225 solar cell as the fabrication process is improved.

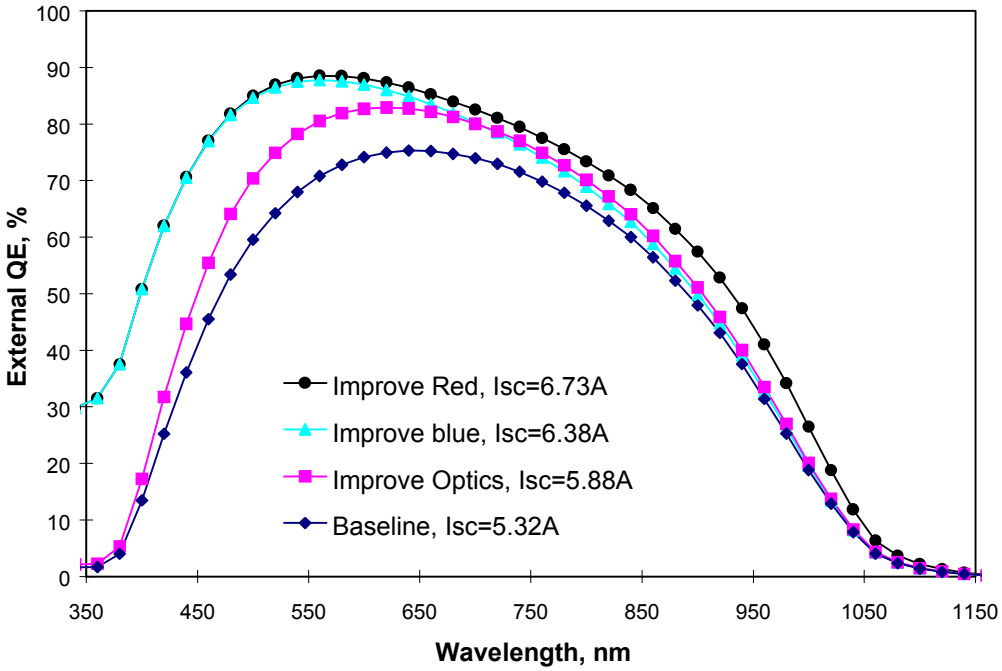


Figure 6. Modeled external quantum efficiencies with proposed improvements.

The conversion efficiency of Silicon-Film™ solar cells has steadily increased since 1987. Figure 7 shows the progression of efficiency and device sizes. The most recent laboratory solar cell has an efficiency of 16.6% as measured at NREL. Full size AP-225 solar cells (240 cm^2) have demonstrated an efficiency of 12.5%, and present production efficiency of the AP-225 solar cell is 10%. Table 3 lists the improvements in Silicon-Film™ performance that are expected to be realized as the production process is improved. All the improvements in Table 3 have been previously demonstrated in Silicon-Film™ solar cells

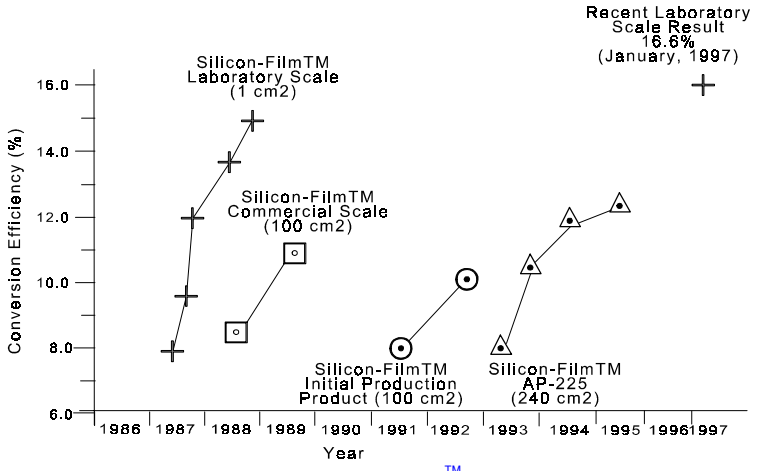


Figure 7. The efficiency history for Silicon-Film™ solar cells.

Table 3.
Proposed improvements in Silicon-Film™ solar cells

Area for Improvement	I_{sc} (A)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	Power (W)	η (%)
Present case (improved optics)	6.31	26.3	0.539	71.8	2.44	10.14
Improved Blue response	6.98	29.1	0.542	72.3	2.74	11.36
Improved FF	6.99	29.1	0.547	75.3	2.88	11.97

The blue response of a typical Silicon-Film™ solar cell is lower than the present industry standard. Blue response, the ability to convert photons at the high energy end of the solar spectrum to usable charge carriers, is sensitive to the specifics of the junction and to passivation of the silicon surface. The electrical resistance of the metal contacts to the diffused layer is also sensitive to the specifics of the junction diffusion. The speed with which the AP-225 was taken to production required the use of a simple junction design and diffusion process to enhance contact conductivity. The path to improved response is extensively detailed in the literature. Improved blue response requires optimization of the diffusion design to minimize contact resistance, and incorporation of surface passivation. The latter can be done as part of the antireflection coating.

Diffusion length represents the single largest area for improvement for Silicon-Film™ material. Several efforts have been undertaken to explain the presence of long diffusion lengths that occur sporadically in Silicon-Film™ as-grown material. Diffusion lengths as high as 200 μm in as-grown material have been measured, with many readings in the 100 to 200 μm range. Achieving 200 μm diffusion lengths will result in production efficiencies of 16.3%.

The fill factor improvements shown in Table 3 highlight several device issues such as contact resistance and imperfect isolation. The leakage current (J_{02}) is associated with defects in the space charge region of the diode. All of the characteristics spelled out in Table 3 have been demonstrated at their target values in full size production solar cells that have been fabricated

with advanced processing. For example, the leakage current (J_{02}) has been reduced to the target level by reducing the surface texture and modifying the junction diffusion.

Advanced Processing Work and Results

Optimization of Solar Cell Optics

The objective of the work performed under this Task is to develop advanced processing techniques that increase the efficiency of production Silicon-Film™ solar cells. This report summarizes the work performed during Phase I to enhance solar cell performance by optimizing production processes related to module and device optics. Work in this area is currently focusing on:

- Reduction of gridline width
- Optimization of AR-coating thickness and index of refraction
- Texturing of the wafer surface for improved light-trapping

Reduced Gridline Width

A video monitoring system has recently been installed in the Silicon-Film™ production facility. This system has been designed to assist the front contact metallization operators in routine monitoring of AP-225 gridline height and width. Previously, this critical step was performed with a simple optical microscope. This new system effectively decreases the time required for gridline inspection by a factor of two. Also, the video system allows operators supervisors, and engineers to view potential defects simultaneously. This new system has improved communication between technical and operating personnel resulting in greater throughput, less downtime, and greater precision and control in Silicon-Film™ research device processing.

Optimized AR-coating Thickness and Index of Refraction

Optimal AR-coating layer parameters (thickness and index of refraction) have been predicted for both encapsulated and un-encapsulated cases. Reflection properties of TiO_2-coated Silicon-Film™ surfaces are being evaluated and the deposition conditions are being tuned to target the optimal thickness and index to achieve minimal reflection losses.

Figure 8 shows reflectance and IQE data for a typical AP-225 solar cell as well as IQE of an AP-225 solar cell with improved blue response. Due to the short diffusion length of AP-225 solar cells it is important that the reflectance minimum of the AR-coating is matched to the peak of the IQE. From Figure 8 it is clear that the solar cell with improved blue response needs a thinner AR-coating than the standard AP-225 solar cell. A thinner AR-coating will shift the minimum of the reflection curve to lower wavelengths, agreeing better with the maximum of the IQE curves.

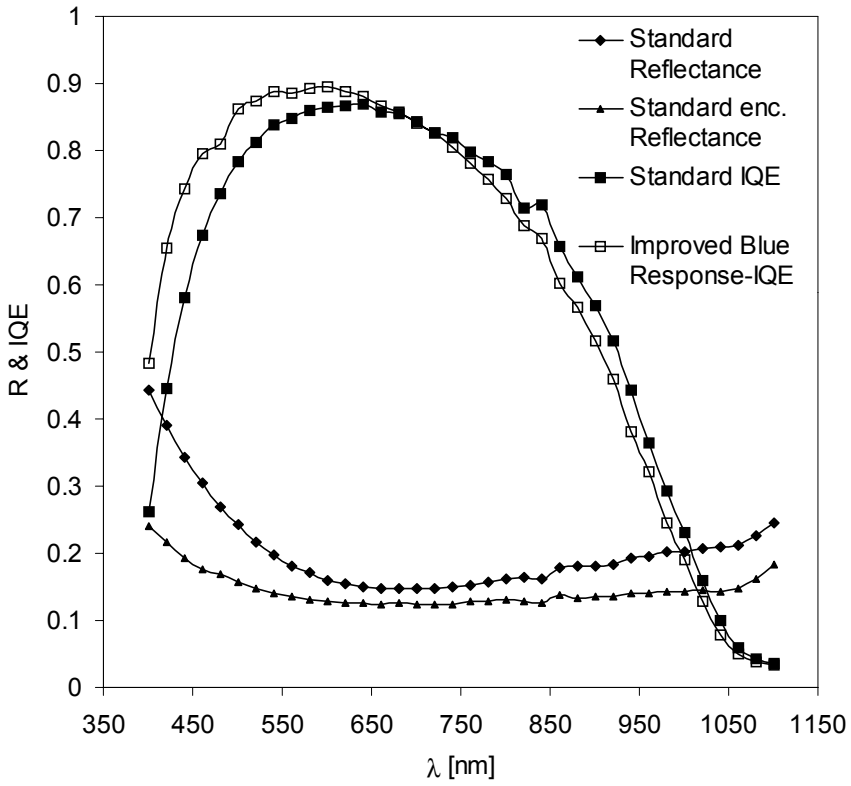
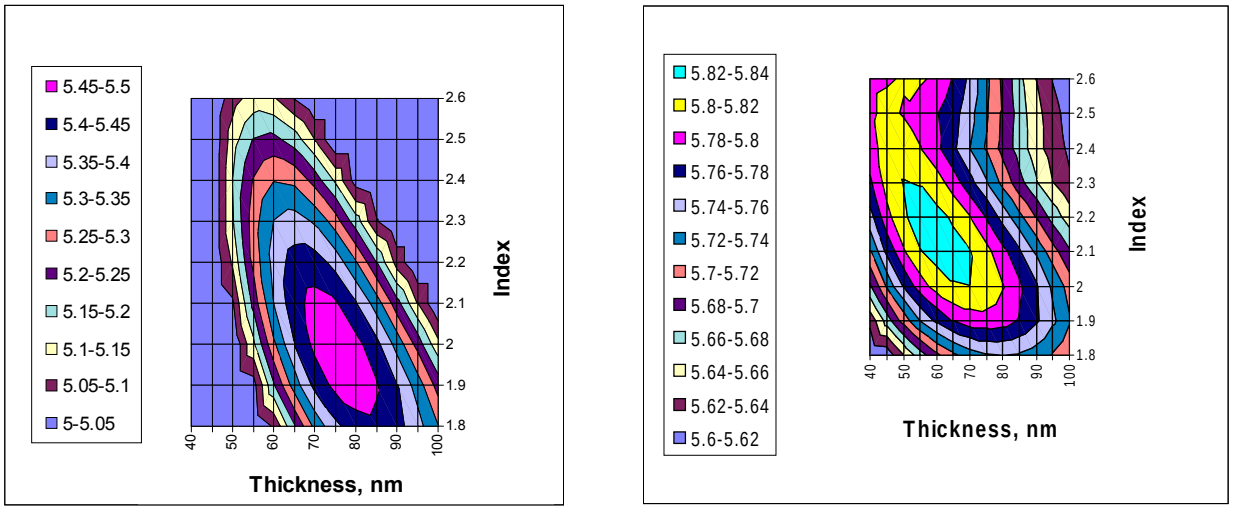


Figure 8. IQE and reflectance of AP-225 solar cells.

To find the optimum thickness and index of refraction for Silicon-Film™ solar cells, the integrated current for an AP-225 solar cell with an IQE as shown in Figure 8 has been calculated as a function of index of refraction and thickness of the AR-coating. Figure 9 shows the results of those calculations for both the encapsulated and the un-encapsulated cases.



Un-encapsulated Encapsulated

Figure 9. Relationship between AR-layer refractive index/thickness and AP-225 short-circuit current.

Using the optimal calculated AR-coating index of refraction and thickness as a starting point, experiments were conducted on small (8 cm^2) pieces of Silicon-Film™ material. To determine thickness and index of refraction, pieces of polished CZ material were coated simultaneously and used for ellipsometry measurements. Encapsulation was simulated by coating the sample with an oil whose refractive index is equal to EVA (used in modules as encapsulant), and by covering with a glass slide. Calculations indicate that the maximum current after encapsulation occurs with an AR-coating thickness of 60 nm and an index of refraction of 2.15. Before encapsulation, a 75 nm AR layer with a refractive index of 2.00 is calculated to yield the lowest solar- and IQE-weighted reflectance (SIWR). The experimental results, however, show that a higher index of refraction (2.4 to 2.5) yields the best results after encapsulation. This is in conflict with the model and may be due to the random texture of Silicon-Film™ material that could not be included in the calculations. Figure 10 shows encapsulated and un-encapsulated SIWR as well as encapsulation gain as a function of index of refraction.

It appears that for the un-encapsulated case the experimental results agree with the model. However, on Silicon-Film™ material, encapsulation gain is strongly dependent on the index of refraction and assumes negative values for $n < 2.25$. The optimum index of refraction according to the experimental results is 2.48.

Further optimization of the AR-coating can be achieved by matching the thickness of the AR-coating to the spectral response of the Silicon-Film™ solar cell. For the standard AP-225 solar cell (see Figure 8), the optimal thickness was found to be about 60 nm (see Figure 11). This number will have to be reevaluated as front surface passivation and improved red response are implemented in AP-225 solar cell production.

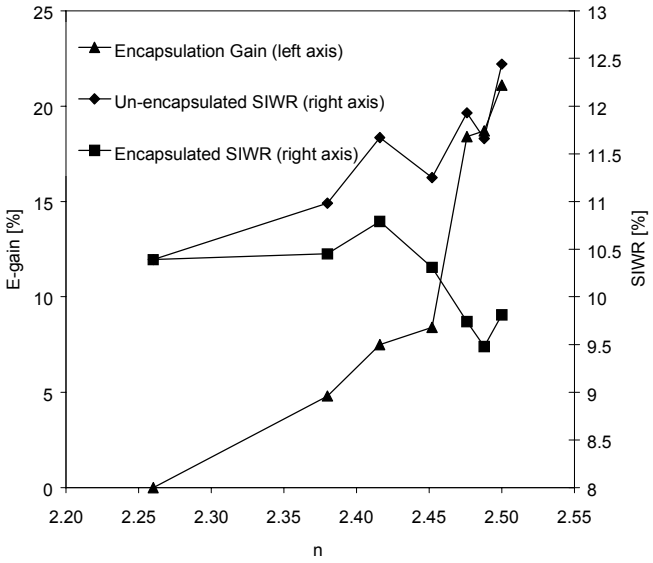


Figure 10. Measured SIWR and encapsulation gain for AP-225 solar cells.

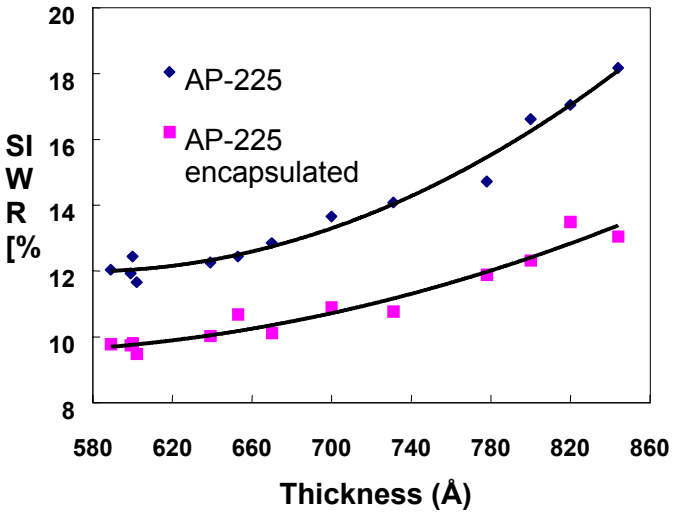


Figure 11. SIWR versus thickness of AR-coating.

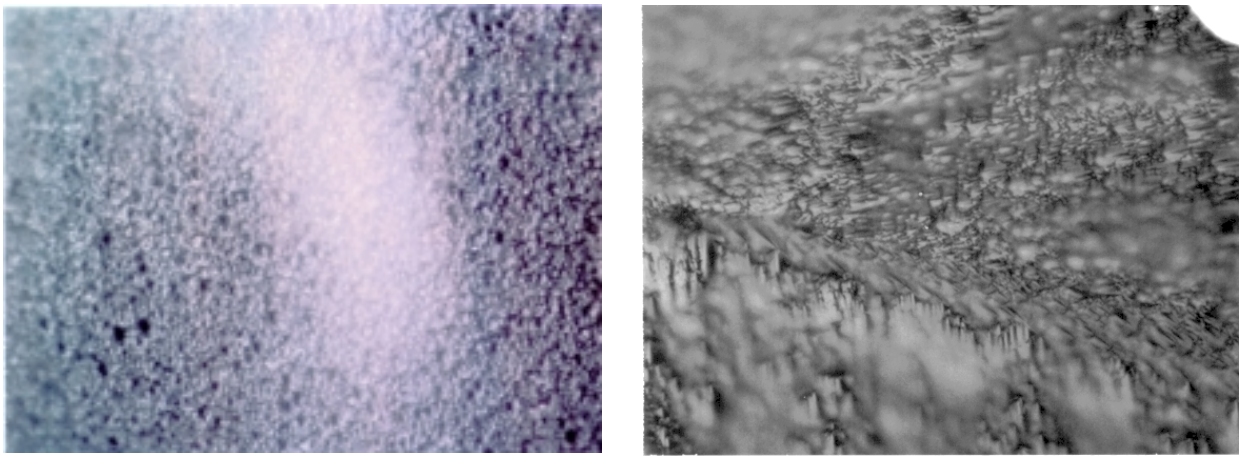
Texture Etch

Chemical texture etching is being considered as a method to decrease cell reflectance and increase light-generated current. A decrease in reflectance can be attributed to the light-trapping between the textured surface and air/glass interface (for encapsulated samples). Several etch chemistries and sequences have been evaluated for both single crystal and Silicon Film™ samples. This additional processing step could be added to both the single crystal and Silicon Film™ production lines if proved successful.

There are two approaches to altering the silicon surface with chemical etching: (1) using an HF/HNO_3 etch to produce a porous silicon layer, and (2) using various etches to alter the topology of the silicon surface. The major drawback of the first approach is the fragile nature of the porous layer. It is not likely to withstand the high temperature post-etch processes. To prevent any damage to the porous layer, the texture etch would ideally be the final step in the solar cell process. As the integrity of the front and back contacts may be compromised by the texture etch, it is not feasible to add wet chemical process steps after cell printing.

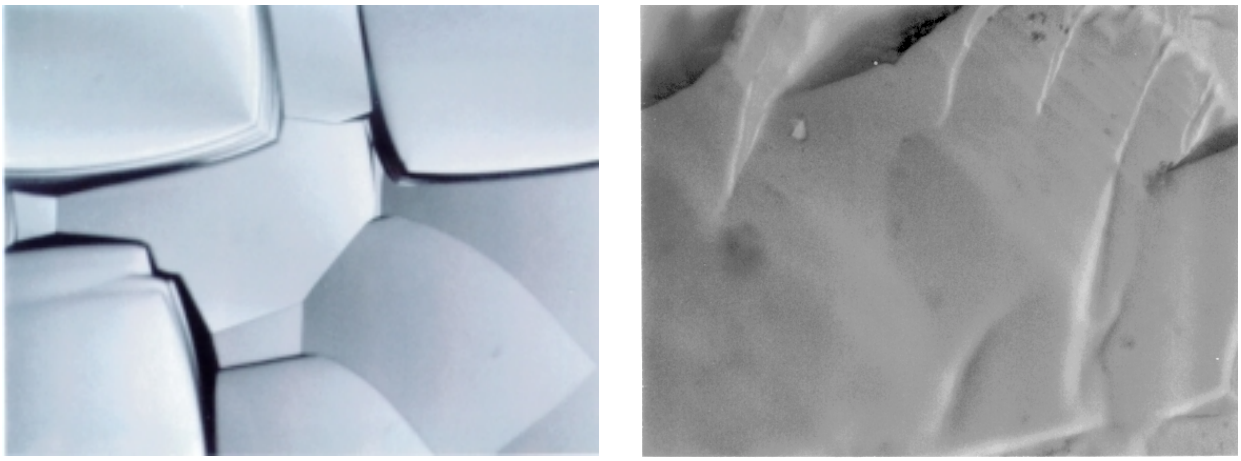
For these reasons, the second approach to chemical texturing of the silicon was given more consideration. The objective was to produce a surface topology that decreases the total reflectance. Three texture chemistries were evaluated: various $HF:HNO_3$ solutions; NaOH followed by $HF:HNO_3$; and NaOH:IPA.

Figure 12 shows a photograph of a single crystal textured wafer. A photograph of a standard surface preparation process etched wafer is shown in Figure 13. Textured Silicon-Film™ samples were slightly darker than the untextured control sample. Not all crystal orientations were textured to the same extent. A highly textured grain surface is shown in Figure 12 (untextured control sample shown in Figure 13).



a. b.

Figure 12. Single crystal (a) and Silicon-Film™ (b) samples after NaOH/IPA texture etch (1000X).



a. b.

Figure 13. Single crystal (a) and Silicon-Film™ (b) control samples (200X).

The resulting reflectivities are shown in Figure 14. Pre-processing did not influence the effectiveness of the etch on single crystal samples; however, Silicon Film™ samples showed lower reflectance after pre-processing. The major drawbacks to the NaOH/IPA texture etch are the extremely long etch time and use of organic solvents.

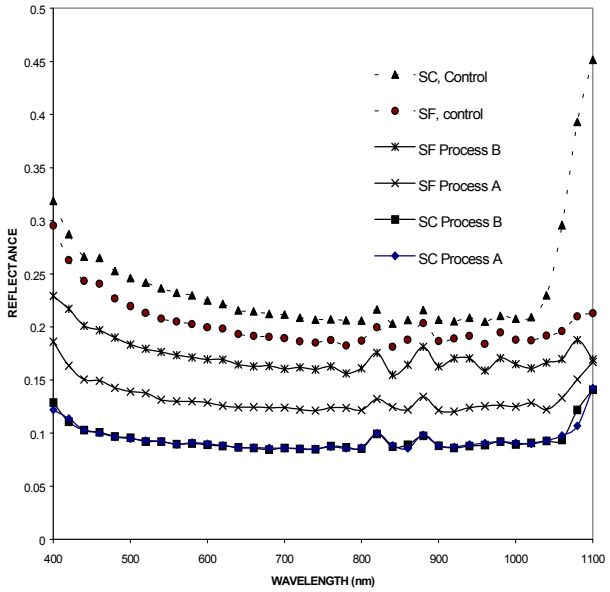


Figure 14. Reflectance measurements for un-encapsulated samples (no AR, SC = single crystal, SF = Silicon-Film™).

Three major areas of possible improvement have been determined and addressed in manufacturing. Gridlines of AP-225 solar cells are now closely monitored and kept at a minimum width. The optimal AR-coating thickness and index of refraction have been experimentally determined. In addition, AR-coating system operators have been trained to use a spectrophotometer, in addition to visual inspection, to closely monitor the quality and thickness of AR-coating. Texture etch experiments have produced some positive results but it has not yet been implemented in production.

Increased Blue Response

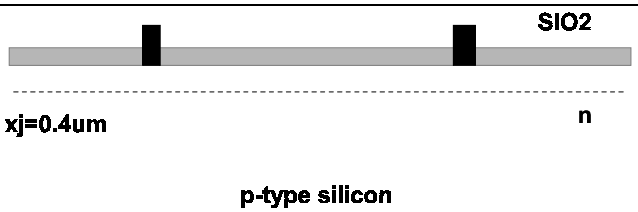
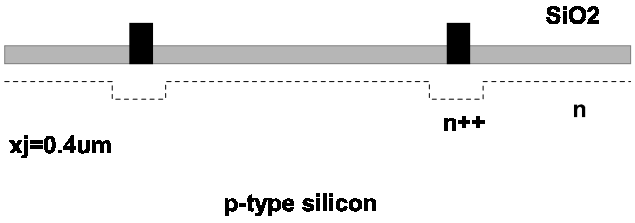
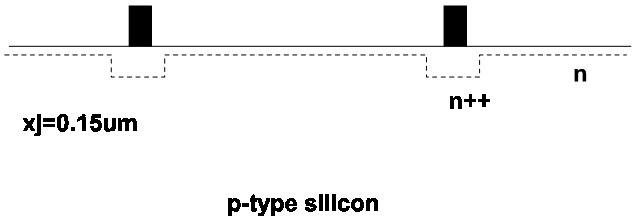
Work in this area is centered on developing a proper combination of junction diffusion and surface passivation processes and optimization of the front screen-printed metallization process. Improvements in the blue response of AP-225 solar cells represent about one third of the potential power which can be gained as the device is optimized.

Two options were considered: a homogenous emitter and a selective emitter (Table 4). These options have different implementation tradeoffs. Our present approach is to combine the emitter diffusion and thermal oxide passivation. The resulting contact resistance and junction leakage problems will be solved through the use of improved front contact pastes and firing conditions. For the homogenous emitter, metallization is the key, requiring selection of the proper silver ink and optimization of the firing conditions. For the selective emitter, a heavier and deeper doping profile needs to be in place below the contact metallization to minimize both junction shunting and contact resistance.

To evaluate the selective emitter concept for Silicon-Film™ materials using belt diffusion processes, an experiment was performed using full size AP-225 wafers with low sheet-resistance diffusions. This experiment was divided into four groups: standard belt diffusion, double

diffusion (twice through the belt), triple diffusion, and finally quadruple diffusion system. Solar cell I-V measurements indicated that an increase in phosphorus doping, decrease in sheet-resistance with each diffusion pass, resulted in a large increase in fill factor, as indicated in Figure 15. This result provides direct experimental evidence that the implementation of selective structures on AP-225 solar cells will result in higher fill factors. The decrease in the short-circuit current is attributed to the decrease in solar cell blue response as the result of increased doping level and junction depth, supporting the need for a selective emitter.

Table 4. Emitter Structures Implementable on AP-225

Option	Schematic	Comment
Homogenous Emitter		1. Simple and easy to implement 2. May have R_s and R_{sh} problems
Selective Emitter (with SiO_2)		1. Has tolerance to mis-alignment of contacts 2. Has control over R_s and R_{sh}
Selective Emitter (without SiO_2)		1. Simpler to implement than selective emitter with SiO_2 2. Has control over R_s and R_{sh} 3. Does not tolerate mis-alignment of contacts

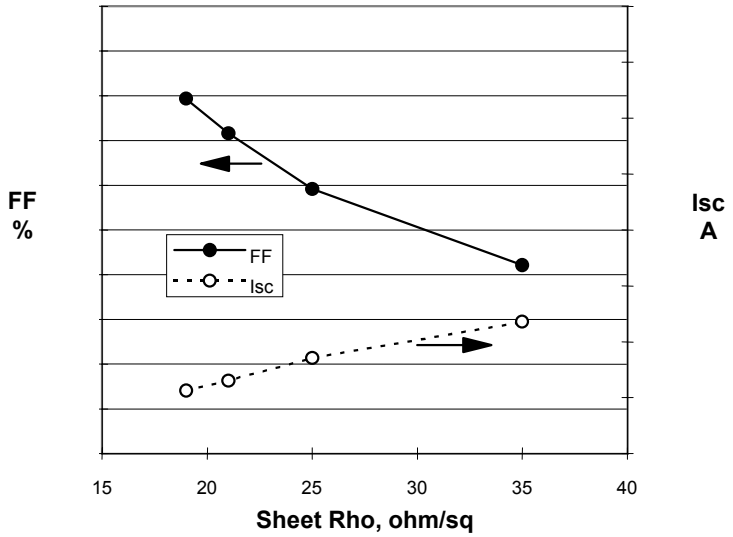


Figure 15. Average solar cell fill factor (FF) and average short-circuit current (I_{sc}) as a function of sheet resistivity.

In manufacturing, the homogeneous emitter approach is easiest to implement. Our recent efforts in improving solar cell blue response have concentrated on belt diffusion, belt oxidation and screen-printed metallization optimization using this structure. Figure 16 illustrates a result achieved on full size AP-225 solar cells with continuous belt-diffusion and tube-oxidation. The estimated short-circuit current gain from surface passivation ranges between 310 mA and 340 mA (after an AR coating is applied). The most promising part of this work is the demonstration of surface passivation effects on material with relatively low sheet resistivity. This work has moved to optimization of a "fire-through-oxide" metallization process and investigation of a continuous surface passivation scheme based on belt-furnace processes.

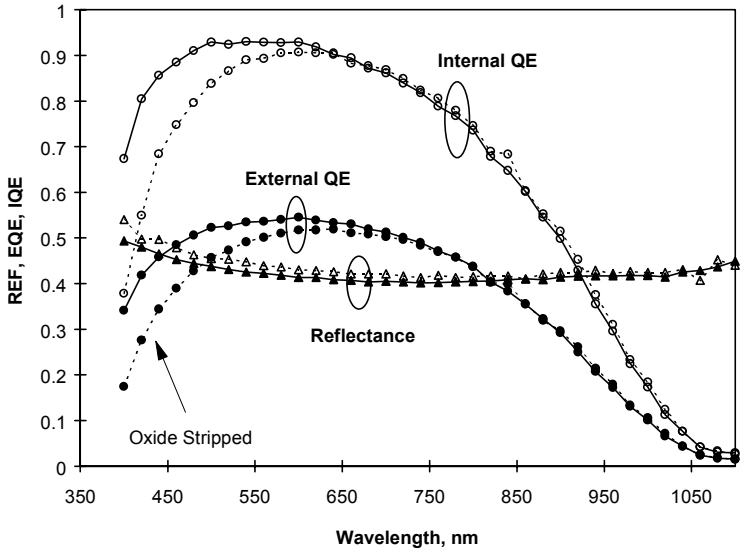


Figure 16. Demonstration of surface passivation on AP-225 solar cells using continuous belt-diffusion.

Optimization of Silicon-Film™ Red Response

We are using both small- and large-area device structures to better understand the solid state phenomena (increases in effective carrier diffusion lengths, shifts in material bulk resistivities, and an increased injection dependence of effective carrier diffusion lengths) that occur during gettering and annealing. We are attempting to understand the relationships between heat treatments and microscopic changes in Silicon-Film™ material. As a part of this effort, we are performing microscopic characterizations of heat-treated materials.

Silicon-Film™ samples were subjected to different high temperature treatments (anneal and getter) and sent to NREL for characterization (FTIR, SIMS, DLTS and lifetime measurement). FTIR analyses indicate that there is a reduction in interstitial oxygen content after high temperature treatments (anneal and getter). These data indicate that improved gettering efficiency could arise from a reduction in oxygen content.

Variability in bulk resistivity has also recently been identified as being related to heat treatment. After high temperature (900°C) heat treatments, Silicon-Film™ bulk resistivity has been found to increase by a factor of 3 to 5. Hall measurements on both as-grown and gettered

Silicon-Film™ material indicate that this resistivity increase is primarily due to a reduction in carrier mobility. The cause of this is not yet clear. More interestingly, as indicated by Dr. Richard Ahrenkiel at NREL, low temperature (~210°C) quench treatments also result in an increase in bulk resistivity. Dr. Ahrenkiel has proposed that this behavior is related to the dissociation of Fe-B pairs in Silicon-Film™ material.

Module Cost Reductions

The objective of work performed under this Task is to reduce the cost of materials and processes associated with Silicon-Film™ module fabrication. Development efforts by AstroPower during Phase I of this contract were focussed primarily in three areas:

- Reduction of the cost of the junction box (J-box) assembly and the assembly time;
- Reduction of the assembly time required to make the electrical connection between the J-box and the laminate; and
- Reduction of the cost of the back sheet material.

AstroPower's new Pencader facility (Newark, DE) for manufacturing solar cells and for module assembly was dedicated in March 1998. A semi-automated tabber-stringer system was purchased and commissioned for this facility, as was a large-area laminator. Additional UL approvals for Silicon-Film™ module and panel products were obtained. Cooperative work between AstroPower and Evergreen Solar on module material cost reductions was postponed until a later date at their request.

The overall goal of the PVMaT-5A program at AstroPower is to engineer and develop flexible manufacturing methods and equipment to process Silicon-Film™ solar cells and modules. While primary emphasis has been placed on wafer and solar cell manufacturing areas, there are areas where incremental and significant improvements have been realized in Silicon-Film™ module design and manufacturing. Specifically, producing a frameless module eliminates the significant cost of the framing materials and the labor required to assemble it. Depending on the cost of the particular components used, the skill of the assembler, and the type and quantity of fixtures and tools, this one change can impact the cost of high power modules by $0.25 per watt (the impact on lower power modules is even greater). Other significant cost reductions have been realized by qualifying lower-cost commercially available bypass diodes that replace custom-fabricated diodes. This has netted savings in the range of $12 to $14 per module. The most time-consuming step in module assembly is the cell stringing operation. Although difficult to implement, automation of this operation will yield significant savings. Other improvements have been realized by purchasing or developing special tools and fixtures. For example, the RTV adhesive (for J-box attachment) is dispensed using pneumatic guns which result in faster, more uniform application. In addition, frame components are now assembled using pneumatic ram tools that replace mallets. These improvements, while incremental, eventually lead to automated assembly techniques as the scale of the module assembly operation increases.

Junction Box

During Phase I of this contract, development efforts were focussed on the J-box assembly. One goal was to design and to qualify a new J-box that incorporates features identified by our customers as essential or desirable. A necessary feature is an electrical feedthrough sized for a 1/2" conduit. A desirable feature is a J-box cover that seals without an O-ring. Other objectives of this project were to reduce the cost of the assembly components by a factor of two, and to secure a local supplier of the box. These objectives could only be achieved by designing our own J-box. We approached several companies who produce injection-molded electrical components (such as electrical boxes, connectors, and terminal blocks) to determine their interest in building the molding tool, producing branded J-boxes for AstroPower, and producing unbranded boxes for other PV module manufacturers. None of these companies saw this as a viable business opportunity. As a result, in addition to designing the J-box, it was also necessary for us to purchase the molding tool and to find a molder to produce the boxes. These tasks were completed during Phase I.

The previous UL-approved J-box assembly for AstroPower modules consists of fourteen components. The most expensive part is a printed-circuit-card assembly that holds the diodes and terminal block. The printed circuit card, J-box, and cover, together with the sealing plugs for the electrical (wiring) feedthrough holes, comprise about 70% of the total cost of the J-box assembly. In addition to the high component cost and significant assembly time, the present J-box has a number of problems and limitations. It is not manufactured within the U.S., which complicates ordering and increases the shipping cost. Also the internal volume of the box, while sufficient to meet UL requirements, makes wiring difficult. Finally, attaching the tabbing to the printed circuit card now requires soldering and is not readily adaptable to automated processes such as welding. Because of these limitations, an effort was made to design and produce a new J-box that would reduce both component cost and assembly time.

The following goals for a new J-box assembly were proposed:

- The injection-molded J-box must be locally produced to reduce uncertainties in supply and quality.
- The assembly should significantly reduce the component cost and the assembly effort. We believe that a 50% reduction is possible.
- The new box should minimize UL-approval requirements.
- The new J-box must be compatible with all existing AP module and frame designs.
- The new design must retain all of the desirable features of our present J-box assembly.

In order to significantly reduce the component cost, we chose to eliminate the printed circuit card in the new J-box design. Instead, a terminal block will serve both electrical and mechanical support functions. The J-box will be molded with electrical feedthrough knock-outs to eliminate the four rubber conduit plugs. The O-ring between the cover and the box lip will be eliminated. Two rather than four cover screws will be used. Tinnerman nuts will be eliminated.

With additional testing and qualification, the cost of the J-box may be further reduced by using a lower cost material such as ABS in place of the polycarbonate plastic.

In order to reduce assembly time, soldered connections between the terminal block and the laminate tabs will be replaced by welded connections. Permanent factory connections on the terminal block will be made using rivets instead of screws. If possible, the terminal block will be purchased as a fully integrated assembly. To eliminate the Tinnerman nuts, the terminal block assembly will be attached to the J-box by heat "staking". Welding, riveting, and heat staking are all operations that can be easily automated with simple tooling. Since the J-box will be molded with electrical knockouts, the new J-box will be used as-received with no further machining or assembly required.

To minimize UL-approval requirements, the J-box will be molded from materials that have already been approved and will use only UL-required components. Thus it will only be necessary to obtain UL approval for the new electrical knock-out feature and for the spray test.

During Phase I a new J-box was designed that met all of the initial goals and should be capable of meeting additional requirements. The new J-box is produced from AstroPower owned tooling by an injection molder on the East Coast. The initial version of the new J-box assembly consists of the following components:

- J-box, cover, and cover retainer to capture the cover to the J-box;
- Four hole plugs to seal the electrical conduit feedthrough holes;
- Two stainless steel cover screws;
- 600-V terminal block;
- Two 8-Amp Schottky bypass diodes.

Presently we are using module string bypass diodes that are rated for 8 amps. Higher current diodes will be required as the area of the Silicon-Film™ solar cell increases. Diodes rated at 10 amps have been procured and are under evaluation using the IEEE-1262 bypass diode thermal test requirements.

At the end of the Phase I effort, the new J-box design was completed and prototype quantities of the new boxes were fabricated. These prototypes are presently undergoing life cycle testing. The new box will be introduced to customers in Phase II.

Laminate Material Cost Reductions

Silicon-Film™ modules are fabricated using tempered glass superstrates. The solar cells are encapsulated using an ethylene-vinyl-acetate (EVA) copolymer. The EVA is protected by a backsheet that consists of a Tedlar™ film laminated to a polyester sheet and a thin sheet of EVA. Due to increased usage of wide (26-inch) back sheet material for large area modules, including Silicon-Film™ modules by AstroPower and our solar cell customers, the supplier of the Tedlar™ sheet material has improved their process to efficiently produce wider rolls. The cost (in $\$/ft^2$) of 26-inch wide Tedlar™ sheet is now comparable to the cost of the narrow (16-inch wide) Tedlar™ sheet. This has resulted in a savings of about $0.01/W for Silicon-Film™ modules.

A glass matting ("scrim") layer had previously been used to allow fast-cure EVA to be used with small-area laminates in a large-area laminator. We have found that this material is not needed to produce large-area laminates in the new laminator. Scrim has been eliminated from the Silicon-Film™ laminates, producing a savings of about $0.01/W in materials per module. Further savings are realized since the purchase and assembly labor involved (cut, place, trim) have been eliminated.

UL Approval

We currently have 20 module products listed with the Underwriters Laboratory (UL). These products include the following Silicon-Film™ modules: APX-40, -45, -75, -80, -85, and -90; and the LAPX-300 frameless panel product.

Module Manufacturing Tools

A SPI-STRINGER™1000 system for fabricating strings with AP-225 Silicon-Film solar cells was procured and commissioned. Finished strings of cells consist of one to ten solar cells that are electrically interconnected in series (front to back). Each solar cell has two bussbars. Solder-coated tabbing strips are automatically placed onto the cells and reflow-soldered to the solar cell bussbars using "no-clean" flux. This is the second tabber-stringer system procured from Spire. Previously we found that the large area and increased thermal mass of the Silicon-Film™ solar cells significantly impacted the throughput of the system. The new system incorporates a larger area heating platen, which increased the pre-heating time so that the residence time at the reflow station was decreased. The system incorporates a semi-automatic wafer feed system. An operator places a solar cell on a target; then a pick-and-place mechanism picks up the cell and places it into the stringer. Completed strings are picked up by an operator and placed in the layout station. Best case throughput improvements of a factor of two have been realized. Because the platen heater has been re-designed, the reliability has also increased, although further improvements remain to be realized.

A large-area laminator for laminating Silicon-Film™ modules was procured from NPC and commissioned in the Pencader facility. This laminator contains a "pin support device", a feature unique to the NPC laminator, that should provide a wide process window with fast-cure EVA, and gives this laminator a potential performance advantage in processing more advanced rapid-cure materials. The platen area of this laminator is 140 cm by 200 cm, and Silicon-Film™ modules of up to 66 cm by 148 cm have been fabricated. Large-area Silicon-Film™ modules with AP-225 solar cells are routinely produced using this laminator. The reliability of this system has been very good, and the major service interval has been lengthened due to improvements in the vacuum pumping system.

Test Equipment Development

QC Tool

Solar cell short wavelength response is typically evaluated using spectral response measurements to obtain internal quantum efficiency. At AstroPower this measurement is performed using chopped broadband light, a monochrometer to select the wavelength, and a lock-in amplifier to obtain the light-generated current. This technique is complicated, tedious and time consuming; a typical set of measurements takes a trained technician or engineer several hours in the laboratory. As a result, spectral response measurements are made only occasionally and on selected samples. It is not possible to test many cells, and the system cannot be used by an operator as a QC tool.

Development of improved emitters and diffusion process control requires a simple, rapid measurement tool so that an operator can easily make in-line measurements. During Phase I we began to develop new measurement methods and systems to accomplish this. One possible approach is based on a cell-to-cell comparison of current generated across several optical passbands by using colored glass filters together with a broadband light source.

Another approach is based on a series of short-wavelength narrowband interference filters that are rapidly changed. If the filters are changed fast enough then the light intensity will be effectively modulated in a manner equivalent to chopping. Measurements of photocurrent are made as each filter passes in front of the light source. The challenges with this approach are: (1) the need to measure a very small modulated current is the presence of the large "ambient" photocurrent due to room light, and (2) the need to process large amounts of data. The advantages are that a quick measurement can be made on the production floor, rather than in the lab, and that the result can be rapidly fed back into the process. Such a system has been designed and is now in the prototype development stage.

Solar Cell IV Testing

During Phase I, a new solar cell tester sorter was designed, constructed and installed in the Pencader facility. This new tester, the CT200, has the following features:

- Access™ database.
- Low-cost CW light source.
- Full IV sweep.
- Menu-driven test and sort parameters.
- Accommodates 8-inch solar cells (AP-400).
- Throughput > 1000 solar cells per hour.

RF-PCD Work and Results

As a continuation of the PVMaT-4a investigation into the RF-PCD technique to characterize Silicon-Film™ sheet material, AstroPower sent a small set of Silicon-Film™ wafers

to Dr. Richard Ahrenkiel at NREL for testing on his RF-PCD apparatus. These wafers were diffused since it had been proven that "as-grown" data had little relationship with "post-annealed" (i.e. heat-treated or diffused) data.

The wafers chosen were from two different production runs to represent a range of solar cell performance quality. The RF-PCD data taken by Dr. Ahrenkiel spanned a range of mobility and lifetime values. His data again determined that the major difference between "good" and "poor" material is minority carrier mobility, not minority carrier lifetime. The wafers tested into two distinct groups with the better cells having an average mobility twice that of the poorer group, but with minority carrier lifetimes that were nearly equal.

After their return to AstroPower, the wafers were tested on Dr. Ron Sinton's quasi-steady-state-PCD (QssPC) system to determine if this system could differentiate between the two groups of solar cells. The QssPC system was unable to distinguish between them; they all had virtually the same test results.

The I-V test results show that the samples that were tested "good" by RF-PCD had a 89% yield at solar cell final test. The wafers identified as "bad" by RF-PCD had a yield of 29% at final test. Although predictive of final test yield, the requirement to thermally anneal all wafers before the RF-PCD test limits the usefulness of the system for sorting as-grown material in a production environment. AstroPower will continue to use RF-PCD as an analysis tool in experiments involving Silicon-Film™ material. For example, RF-PCD measurements have been helpful in determining the effects of different anneal conditions.

Metallurgical-Grade Silicon for Solar Application

The objective of the work performed under this task is to develop directional solidification methods to upgrade metallurgical grade silicon (MG-Si) for use as a low-cost feedstock material for the Silicon-Film™ sheet process. The approach builds on previously established successes (e.g. Dow Corning, Exxon/Elkem, Siemens, Kawasaki) that used conventional uni-directional solidification (e.g. Czochralski or Bridgman) to purify MG-Si silicon. Each of these groups have successfully employed various metallurgical methods, coupled with directional solidification, to process MG-Si into photovoltaic grade silicon (PVG – Si) from which solar cells with conversion efficiency greater than 10% were fabricated. During the initial phase of this work an existing processing furnace was modified to directionally solidify MG-Si so that the impurities are selectively moved to one surface. This surface was then mechanically removed and the resulting upgraded material was processed into feedstock material for the Silicon-Film™ sheet process. Cross-sections of the purified material were prepared for the purpose of measuring the linear impurity profile by SIMS. A key element in this task is the identification of metallurgical grade silicon vendors that can supply feedstock with low boron concentrations, as directional solidification is ineffective for this element.

The poly-Si feedstock supply for silicon photovoltaics is presently based entirely on the by-product stream generated by the semiconductor device industry. The method for generating poly-Si for the semiconductor industry (SG-Si) is based on the Siemens process which converts metallurgical grade silicon (MG-Si) into purified poly-Si. The price of SG-Si is $45/kg to

$60/kg. The total by-product stream available for PV amounts to about 10% of the SG-Si production rate or approximately 1800 MT (metric tons) in 1998. The by-product silicon is priced between $3 and $20/kg.

Figure 17 details the standard production of metallurgical grade silicon by the carbothermic process, and indicates several approaches used to convert metallurgical grade silicon into solar grade silicon. Decision points Q are employed to qualify an approach based on a specification for solar grade silicon.

Paths 1, 2, and 3 all begin with the carbothermic reduction of quartzite (sand). The product of this process step is called metallurgical-grade silicon (MG-Si). Path 1 capitalizes on the idea of starting with pure starting materials for the carbothermic reduction process. Path 2 is presently the one employed by all the manufacturers of Poly-Si for the semiconductor industry and is reviewed by McCORMICK, 1985 [2]. This path uses the *chemical approach* to purify MG-Si, and is effective at removing boron. However, the costs to effect these processes is typically high (>$30/kg), and accordingly, this path will not be treated in this report.

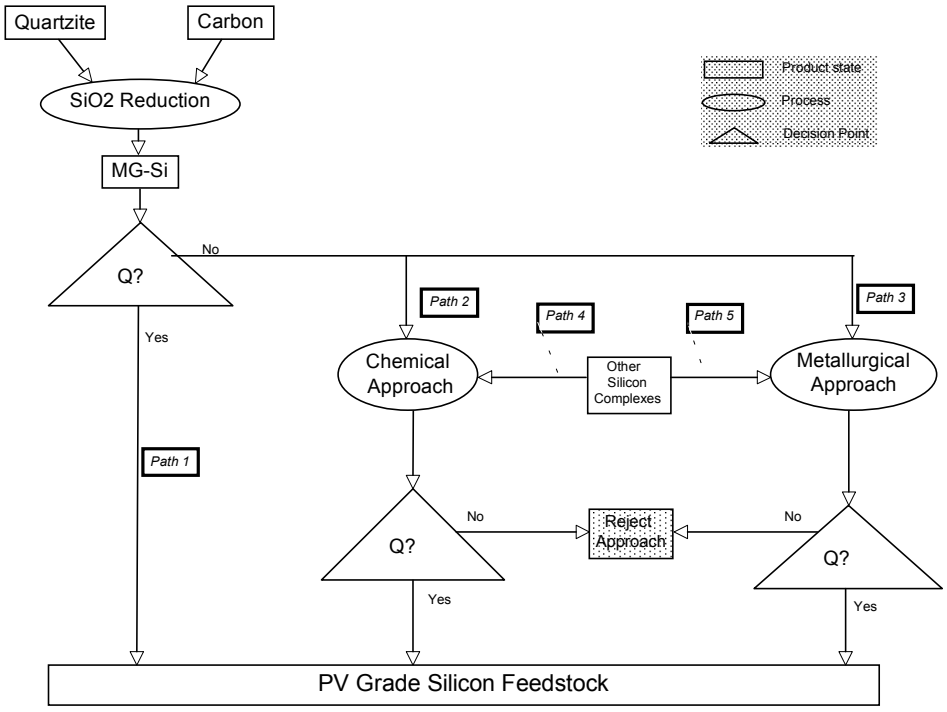


Figure 17. Paths to solar (PV) grade materials.

Path 3 is the *metallurgical approach* (DIETL, 1988) [3] which has the potential to result in a lower cost product (i.e., lower energy expenditure), but which does not deal effectively with boron. Paths 4 and 5 represent alternative non-carbothermic approaches for generating silicon to be subsequently upgraded using either the chemical approach or metallurgical approach.

The metallurgical approach (Path 3) for refining silicon has the potential to result in a lower cost product (i.e., lower energy expenditure). The foremost issue that must be addressed to qualify any metallurgical sequence is dealing with boron.

There are other approaches for supplying silicon for the metallurgical refinement route (Path 5). Metallothermic reduction using aluminum has been investigated at Wacker (DIETL and HOLM, 1987) [4], but requires dealing with the Al_2O_3 by-product in order to recycle the aluminum.

Metallothermic reduction of SiF_4 by Na and $SiCl_4$ by Zn have both been employed to produce elemental silicon. The SiF_4 or H_2SiF_6 (a by-product from the phosphate fertilizer industry) reduction by Na has achieved low boron concentration. The Zn reduction of $SiCl_4$ has been extensively investigated. This process was used to generate the first available "electronic" grade silicon in 1952 (LYON ET AL., 1949) [5]. The more economic Siemens process subsequently replaced it.

Electrodeposition of MG-Si to produce a photovoltaic grade silicon has also been investigated. In general the approach is plagued by the same low linear growth rate (typically 1 to 2 micron/min) that limits the Siemens-based CVD approach, thus requiring very large reaction areas in order to achieve meaningful mass generation rates.

Table 5 lists specific metallurgical methods to achieve low boron silicon feedstock, and indicates the silicon phase to which the methods are applied. Implicit in this plan is the need to employ the methods in a rational sequence to effect the required purification.

Table 5. Purification Methods - Metallurgical Approach

Silicon Phase	Purification Method
Liquid	Starting Materials
	Liquid-Liquid Extraction
	Liquid-Gas Extraction
Liquid/Solid	Segregation
Solid	Solid-Liquid Extraction
	Gettering

The approach for manufacturing silicon feedstock has been well developed for the semiconductor industry, but does not meet the requirements for the production of large amounts of cheap, moderate purity, photovoltaic grade solid-silicon feedstock. The cost for PV grade silicon and for semiconductor grade silicon using chemical processes is essentially the same at $45/kg. Silicon solar feedstock technology has simply been piggybacking on the semiconductor industry for the past 30 years. The development of a large solar power industry requires a cheaper silicon feedstock that does not have the high purity requirements of the semiconductor wafer industry. For even a moderate growth of the solar industry (20% per year), the future supply of silicon feedstock is in question. As the production of semiconductor grade silicon feedstock begins to level off, a major opportunity-cost driven price restructuring will occur for

the whole silicon feedstock industry, and the feedstock cost for silicon solar cells will increase drastically.

The metallurgical approach shows the greatest promise for producing solar-grade silicon. A paradigm for achieving this goal is provided by the steel industry that, over the last forty years, has developed methods which employ comparable processes to produce steel with impurity control at the ppm level. The necessary event is the production of a metallurgical grade silicon with the proper boron concentration level to enable purification by subsequent metallurgical means.

A key element in this task is the identification of metallurgical grade silicon vendors that can supply feedstock with sufficiently low boron concentrations, as directional solidification is ineffective for this element. Several silicon metal vendors have provided sample material for our project, and discussion with industry vendors revealed potential materials that would yield boron concentrations in the 1 ppm range. Table 6 below indicates the impurity levels of several targeted elements that were determined to be present in the material from these sources.

Table 6. Chemical Analysis – Metallurgical-Grade Silicon

	Vendor A	Vendor B	Vendor C	Vendor D	Vendor E
Element	(ppm)	(ppm)	(ppm)	(ppm)	(ppm)
Al	2270	810	1810	120	850
Ca	232	131	6	60	106
Cr	4	3	23	1	8
Cu	2	1	9		
Fe	1280	310	2410	480	790
Mg	6	3	6		
Mn	8	3	31		
Ni	<5	3	7		
Ti	118	20	190		69
V	5	5	17	27	
B	26	25	<50	6	5
P	29	29	12		
O	1000	270			
C	840	1000			

In order to evaluate their suitability, samples of the metallurgical grade silicon were run through the existing processing furnace that had been modified to allow for uni-directional solidification. Initial runs in the machine resulted in ingots that were characterized by NREL using SIMS analysis. A "line profile" was determined by measuring the depth profile of several independent elements at three points (bottom, middle and top) along the direction of solidification.

The elements selected for measurement were aluminum, calcium, chromium, iron, titanium, and boron. Aluminum, calcium, iron, and titanium are typically the most abundant elements reported by the silicon metal vendors for their material. (It is noted that the concentration of carbon and oxygen are significant as well – 200-1000 ppm – but at this time are not being quantitatively followed). Chromium was selected as a flag for stainless steel contamination, and of course, boron is the key to achieving the required electrical properties.

Results indicated that the boron level remained high after the purification step (roughly unchanged), but that the targeted impurities were all reduced in concentration by factors of 88 to over 10,000. Development of this technique will be pursued in Phase II.

Reduce Silicon Consumption through Recycling

A process to effect the recycling of the silicon material resulting from the trimming of Silicon-Film™ sheets during the wafer process, as well as other waste stream supplies, has been designed and an initial apparatus for elevated temperature treatments has been constructed. The apparatus is capable of accepting material of varying geometric shapes and of converting them

into a uniform form factor. Initially, this apparatus will produce a uniform starting material for our powder sizing process, thus enabling the achievement of higher material yield for that step. In the longer term it is anticipated that this apparatus will provide the tool for determining a process to convert variable size inputs to a fixed size output directly compatible with the requirements of the Silicon Film™ sheet machine.

Runs have verified the throughput design features intended. Material processed by the apparatus has been prepared into a Silicon-Film™ sheet, and has yielded solar cells of acceptable performance. It is estimated that this and related processes will bring the material yield of as-received material through the wafer machine to over 95%.

Summary

Phase I progress for the AstroPower PVMaT-5A effort has been discussed. Significant technical progress has been reported in the areas of in-line wet processing, solar cell efficiency and module cost reduction. Continuous metallization requires more development in Phases II and III. A new high-throughput sheet machine is scheduled for fabrication in the first half of the Phase II program.

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13. ABSTRACT *(Maximum 200 words)*
AstroPower is developing a manufacturing process for Silicon-Film™ solar cell production under the Photovoltaic Manufacturing Technology (PVMaT) cost-share program. This document reports on results from the first phase of a three-phase effort. Progress is reported on developing new procedures and equipment for in-line wet-chemical processes, metallization processes, sheet fabrication, solar cell processing, module assembly, solar cell testing, metallurgical-grade silicon purification, and recycling of Silicon-Film™ sheet materials. Future concepts and goals for the Silicon-Film™ process are also discussed.

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